

ABSTRACT OF THE DISCLOSURE

A first processor, a second processor, a memory and a clock supply unit are integrated together on a single chip. The first processor operates synchronously with a first internal clock signal. The second processor operates synchronously with a second internal clock signal. The memory operates synchronously with a third internal clock signal. The clock supply unit generates three clock signals, which are in phase with each other, from an external clock signal and supplies those clock signals as the first, second and third internal clock signals. The first and second processors share the memory via a data bus. Each of the processors has an internal reset signal.